Claims

1. A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly including one or more regions, wherein at least one of the regions is an oxide region;

exposing a surface of at least the oxide region to a nitrogen containing atmosphere resulting in a passivation layer on the surface of the at least one oxide region;

forming a layer of a metal material over at least the passivation layer; and

thermally treating the substrate assembly, the passivation layer substantially preventing formation of an interfacial metal oxide between the metal material and the oxide region.

2. The method according to claim 1, wherein the nitrogen containing atmosphere comprises N_2 or NH_3.

3. The method according to claim 1, wherein exposing the surface of the oxide region comprises exposing the surface of the oxide region to a nitrogen containing plasma.

4. The method according to claim 3, wherein the plasma comprises nitrogen in a range of approximately 10 sccm to approximately 5,000 sccm by volume.

5. The method according to claim 1, wherein performing the thermal treatment comprises performing a rapid thermal process on the substrate assembly.

6. The method according to claim 5, wherein the rapid thermal process is performed at a temperature ranging between approximately 400 °C and

approximately 1,000 °C for a duration of time ranging between approximately 20 seconds and approximately 40 seconds.

7. The method according to claim 1, wherein the passivation layer comprises $Si_xO_yN_z$.

8. The method according to claim 7, wherein the passivation layer has a thickness ranging between approximately 10 Å and approximately 100 Å.

9. The method according to claim 1, wherein the metal material comprises titanium.

10. The method according to claim 9, wherein:

the passivation layer and titanium layer are formed relative to a field oxide region and a silicon substrate region; and

thermally treating the substrate assembly includes salicidation of at least a portion of the silicon substrate region resulting formation of titanium silicide.

11. The method according to claim 9, wherein thermally treating the substrate assembly includes performing a rapid thermal nitridation process resulting in formation of titanium nitride.

12. A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly including at least an oxide region; forming a layer of titanium over a surface of at least the oxide region;

treating the oxide region surface with a plasma comprising nitrogen prior to forming the titanium layer so as to form a passivation layer upon which the titanium layer is formed; and

performing a thermal treatment on the substrate assembly, the passivation layer substantially inhibiting diffusion of oxygen from the oxide layer during the thermal treatment of the substrate assembly.

13. The method according to claim 12, wherein the plasma comprises N_2 or NH_3.

14. The method according to claim 12, wherein the plasma comprises nitrogen in a range of approximately 10 sccm to approximately 5,000 sccm by volume.

15. The method according to claim 12, wherein performing the thermal treatment comprises performing a rapid thermal process on the substrate assembly.

16. The method according to claim 15, wherein the rapid thermal process is performed at a temperature ranging between approximately 400 °C and approximately 1,000 °C.

17. The method according to claim 12, wherein performing the thermal treatment comprises annealing the substrate assembly at a temperature ranging between approximately 400 °C and approximately 1,000 °C in a nitrogen containing atmosphere.

18. The method according to claim 12, wherein the passivation layer comprises $Si_xO_yN_z$.

19. The method according to claim 12, wherein the passivation layer has a thickness ranging between approximately 10 Å and approximately 100 Å.

20. A salicidation method for use in fabrication of an integrated circuit,

comprising:

providing a transistor structure including a gate structure and field oxide regions formed relative to a silicon substrate defining at least one contact area;

forming a passivation layer over at least a portion of one of the field oxide regions using a nitrogen containing plasma;

forming a layer of titanium over at least a surface of the passivation layer; and

thermally treating the transistor structure to form titanium silicide at the contact area, the passivation layer substantially inhibiting diffusion of oxygen from the field oxide region during thermal treatment of the transistor structure.

21. The method according to claim 20, further comprising selectively removing unreacted titanium or titanium nitride against titanium silicide using an aqueous cleaning solution.

22. The method according to claim 20, wherein thermally treating the transistor structure comprises thermally treating the transistor structure using a rapid thermal process.

23. The method according to claim 22, wherein the rapid thermal process is performed at a temperature ranging between approximately 400 °C and approximately 1,000 °C for a duration of time ranging between approximately 20 seconds and approximately 2 minutes.

24. The method according to claim 22, further comprising removing unreacted titanium.

25. The method according to claim 20, wherein thermally treating the transistor structure comprises thermally treating the transistor structure using a rapid thermal nitridation process resulting in formation of titanium nitride over at least the field

oxide region.

26. The method according to claim 25, wherein the rapid thermal nitridation process is performed at a temperature ranging between approximately 400 °C and approximately 1,000 °C for a duration of time ranging between approximately 20 seconds and approximately 2 minutes.

27. The method according to claim 25, further comprising removing unreacted titanium and titanium nitride.

28. The method according to claim 25, further comprising patterning the titanium nitride to form a local interconnect from the titanium silicide over at least one oxide region to another contact region.

29. The method according to claim 20, wherein the nitrogen containing atmosphere comprises N_2 or NH_3.

30. The method according to claim 20, wherein the plasma comprises nitrogen in a range of approximately 10 sccm to approximately 5,000 sccm by volume.

31. The method according to claim 20, wherein the passivation layer comprises $Si_xO_yN_z$.

32. The method according to claim 31, wherein the passivation layer has a thickness ranging between approximately 10 Å and approximately 100 Å.

33. A method for use in forming an interconnect in the fabrication of a semiconductor device, comprising:

providing a substrate assembly including a first contact region, a second

contact region, and an oxide region at a location therebetween;

exposing a surface of the oxide region to a nitrogen containing plasma so as to form a passivation layer;

forming a layer of titanium over at least the surface of the oxide region and the first and second contact regions; and

performing a thermal treatment to form a layer of nitridated titanium extending at least between the first contact region and the second contact region and directly over the oxide region, the passivation layer inhibiting formation of titanium oxide at an interface between the titanium layer and the oxide region.

34. The method according to claim 33, further comprising patterning the nitridated titanium layer to form the interconnect.

35. The method according to claim 33, wherein the plasma comprises N_2 or NH_3.

36. The method according to claim 33, wherein plasma comprises nitrogen in a range of approximately 10 sccm to approximately 5,000 sccm by volume.

37. The method according to claim 33, wherein performing the thermal treatment comprises performing a rapid thermal process on the substrate assembly in a nitrogen atmosphere.

38. The method according to claim 37, wherein the rapid thermal process is performed at a temperature ranging between approximately 400 °C and approximately 1,000 °C for a duration of time ranging between approximately 20 seconds and approximately 2 minutes.

39. The method according to claim 33, wherein performing the thermal treatment comprises siliciding at least one of the first or second contact regions.

40. The method according to claim 33, wherein the passivation layer comprises $Si_xO_yN_z$.

41. The method according to claim 40, wherein the passivation layer has a thickness ranging between approximately 10 Å and approximately 100 Å.

42. A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly comprising one or more regions, wherein at least one of the regions is an oxide region;

forming a passivation layer on a surface of the oxide region;

depositing a layer of metal material over the passivation layer; and

thermally treating the substrate assembly, wherein the passivation layer substantially prevents formation of a metal oxide at the oxide region during thermal treatment.

43. The method according to claim 42, wherein forming the passivation layer comprises exposing the surface of the oxide region to a nitrogen containing plasma.

44. The method according to claim 43, wherein the nitrogen containing plasma comprises one or more compounds selected from the group consisting of N_2, NH_3, NH=NH, and NH_2-NH_2.

45. The method according to claim 42, wherein the passivation layer comprises $Si_xO_yN_z$.

46. The method according to claim 42, wherein thermally treating the substrate assembly comprises performing a rapid thermal process on the substrate assembly at a temperature ranging between approximately 400 °C and 1,000 °C for a duration of time ranging between approximately 20 seconds and 2 minutes.

47. The method according to claim 42, wherein depositing the layer of metal material comprises depositing a titanium layer.

48. The method according to claim 47, wherein depositing the titanium layer comprises depositing the titanium layer to a thickness ranging from about 100 Å to about 500 Å.

49. The method according to claim 42, wherein the layer of metal material is deposited by a process selected from the group consisting of sputter deposition, chemical vapor deposition, physical vapor deposition, thermal evaporation, electron evaporation, and combinations thereof.

50. The method according to claim 42, wherein the passivation layer has a thickness ranging between about 10 Å and about 100 Å.

51. A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly comprising an oxide region and a non-oxide region;

forming a passivation layer on a surface of the oxide region;

depositing a layer of metal material over the passivation layer and the non-oxide region; and

thermally treating the substrate assembly, wherein the passivation layer substantially prevents formation of a metal oxide between the layer of metal material and the oxide region during thermal treatment.

52. The method according to claim 51, wherein forming the passivation layer comprises exposing the surface of the oxide region to a nitrogen containing plasma.

53. The method according to claim 52, wherein the nitrogen containing plasma comprises nitrogen in a range of about 10 sccm to about 5,000 sccm.

54. The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises exposing the surface to a pressure ranging between about 0.1 Torr and about 10 Torr.

55. The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises exposing the surface to a temperature ranging between about 100 °C and about 500 °C.

56. The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises providing power associated with the plasma ranging between about 300 Watts and about 3000 Watts.

57. The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises exposing the surface for a period of time ranging between about 20 seconds and about 600 seconds.

58. The method according to claim 51, wherein depositing the layer of metal material comprises depositing a titanium layer.

59. A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly including an oxide region and a silicon region;

exposing a surface of the oxide region to a plasma comprising nitrogen so as to form a passivation layer over the surface;

depositing a layer of titanium over the passivation layer and the silicon region; and

performing a thermal treatment on the substrate assembly, wherein the passivation layer substantially prevents formation of titanium oxide between the layer of titanium and the oxide region during thermal treatment.

60. The method according to claim 59, wherein the plasma comprises N_2 or NH_3.

61. The method according to claim 59, wherein the plasma comprises nitrogen in a range of about 10 sccm to about 5,000 sccm.

62. The method according to claim 59, wherein performing the thermal treatment comprises performing a rapid thermal process.

63. The method according to claim 62, wherein the rapid thermal process is performed at a temperature ranging between approximately 400 °C and approximately 1,000 °C.

64. The method according to claim 59, wherein performing the thermal treatment comprises annealing the substrate assembly at a temperature ranging between approximately 500 °C and approximately 1,000 °C.

65. The method according to claim 59, wherein the passivation layer comprises $Si_xO_yN_z$.

66. The method according to claim 59, wherein the passivation layer has a thickness ranging between about 10 Å and about 100 Å.

67. The method according to claim 59, wherein performing the thermal treatment comprises performing a rapid thermal nitridation process resulting in formation of a titanium silicide layer on the silicon region.